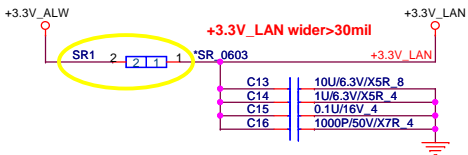


These Caps close to LAN Chip VDD33 pins

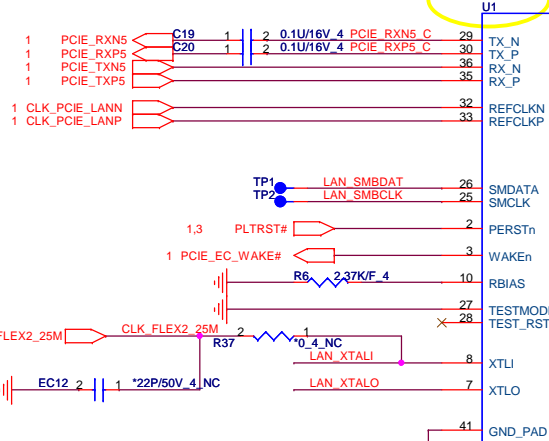


20120204
Change R1 to SR1(SJ0603)

	PN	Footprint	SKU
AR8161	AL008161002	qfn40-5x5-4-41p-0_9h	R08T, V08, V08A
AR8162	AL008162000	qfn40-5x5-4-41p-0_9h	R08, R08A

20120203

Change U1 PN to AL008162001(ver B)



Atheros
AR8161
AR8162

+1.1V_DVDD wider>20mil

+2.7V_AVDD wider>20mil

+1.1V_AVDD wider>20mil

+3.3V_RUN

+1.1V_AVDD

+1.1V_AVDD

+1.1V_AVDD

+1.1V_AVDD

+1.1V_AVDD

+1.1V_AVDD

+1.1V_AVDD

+1.1V_AVDD

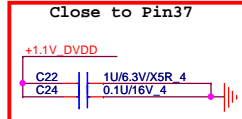
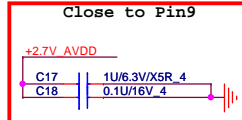
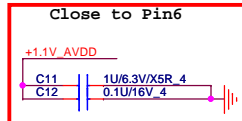
+1.1V_AVDD

+1.1V_AVDD

+1.1V_AVDD

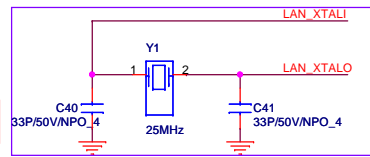
+1.1V_AVDD

+1.1V_AVDD



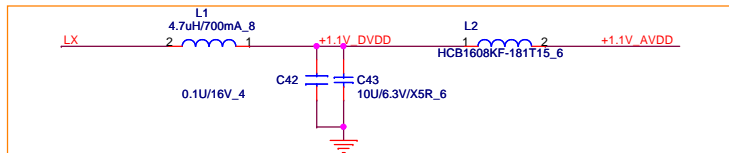
	Crystal BOM
Crystal BOM	POP C40 C41 Y1, NC R37 EC12
PCH clock BOM	NC C40 C41 Y1, POP R37 EC12

LED1 (Pin39)	Regulator select		L1	L2	C42	C43
	LDO	Low	NC	NC	NC	NC
	SWR*	High	V	V	V	V



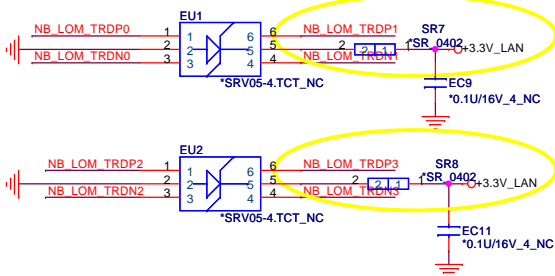
	Over-clocking enable	Over-clocking disable
LED_ACT	1	0

	LDO mode(Default)	SWR mode
LED1	Mount R35	NC R35



LAN Co-lay information

	C45	C46	C47	C48	C27
AR8161	V	V	V	V	V
AR8162	NC	NC	V	V	NC



20120203

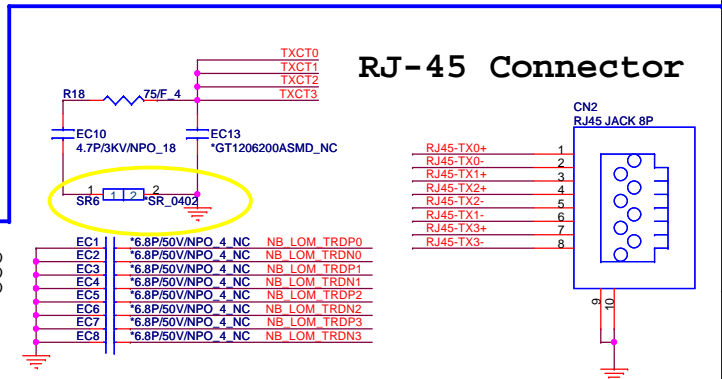
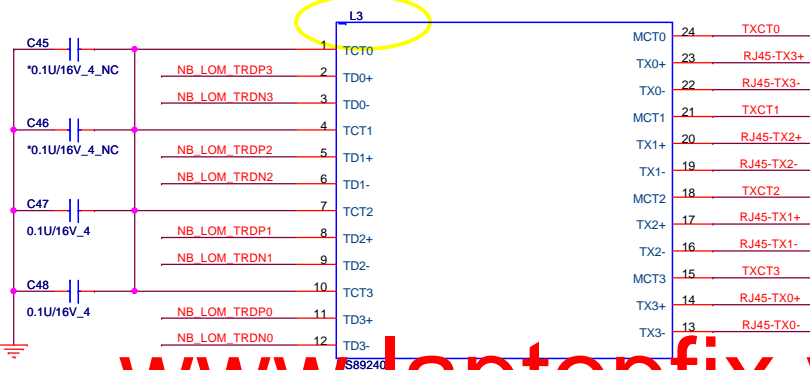
Change L3 to DB0EF7LAN01(FCE)

20120206

Change R58 to SR6(short0402)

Change R14 to SR7(short0402)

Change R19 to SR8(short0402)



Transformer Co-lay information (follow R01)

Mode	L3(transformer)	U1
10/100	NS892408 (DB0EF7LAN01)	AR8162-A
Giga	LF89276C-R (DB0LL1LAN00)	AR8161-A



Quanta Computer Inc.
PROJECT : R08

Size	Document Number	Rev
	LAN (AR8161A / AR8162)colay	A00
Date	Monday, February 13, 2012	Sheet 2 of 4

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[illegible]

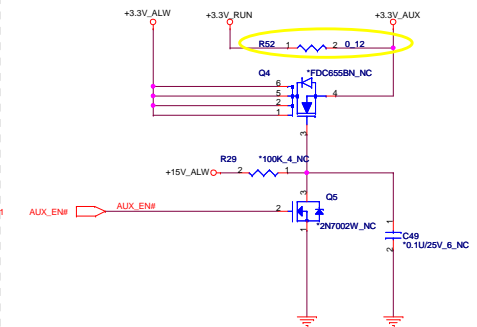
Support AOAC on WLAN

20120204

Change R52 to SR2(short1206)

20120213

Change SR2 back to R52



20120204

Change R54 to SR3 (short)

20120213

Change SR3 back to R54

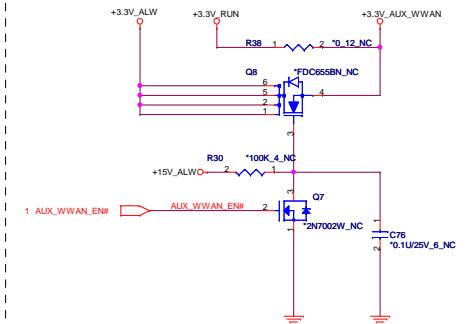
20120206

Remove EL4

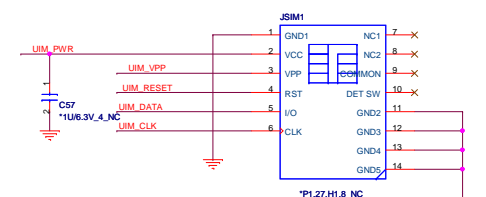
Change R39 to SR4(short0402)

Change R40 to SR5(short0402)

Support AOAC on WWAN

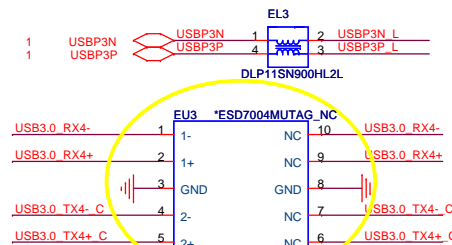
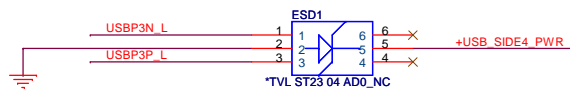
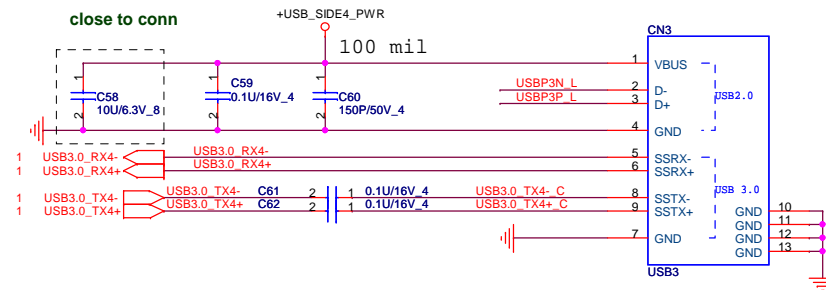
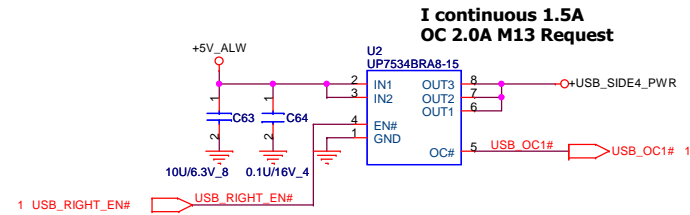


SIM SOCKET



Place as close as possible to JSIM1 connector

Spacing 1:1



ESD Function

20120213
NC EU3